Lecture 20 – The CMOS Inverter

20.1) The CMOS Inverter Circuit and Operation

The CMOS inverter consists of an NMOS and PMOS matched pair. Remember, because the hole mobility is less than that of the electron mobility the width of the PMOS device is larger than that of the NMOS such that

\[ W_p \mu_p = W_n \mu_n \]

Typically, \( W_p \approx 2 \) to 3 times \( W_n \)

When the input is high i.e. \( v_I = V_{DD} \), transistor \( Q_N \) is ‘on’ and \( Q_P \) is ‘off’. The output is therefore connected to ground via the small on-state resistance of pull-down transistor \( Q_N \) i.e. \( v_O = 0 = \text{'low'} \). To understand this consider the I/V curve of \( Q_N \) with \( Q_P \) as the load:

The operating point occurs at the intersection of the two curves, which for this case gives \( v_O = V_{OL} \approx 0V \). The resistance from the output to ground is simply the resistance of \( Q_N \) which we write as \( r_{DSN} \).

Note that \( Q_N \) is in the linear (or triode) regime and hence:

\[
I_D^{QN} = k \frac{W}{L} \left[ (V_{GS} - V_t)V_{DS} - \frac{V_{DS}^2}{2} \right]
\]
For the case when $v_I$ is high then $v_{GS} = V_{DD}$ and $v_{DS} \sim 0$ so that we can neglect $V_{DS}^2$.

\[
\Rightarrow r_{DSN} \approx \frac{1}{k_n \left( \frac{W}{L} \right)_n (V_{DD} - V_{tn})}
\]

Likewise, when the input is low i.e. $v_I = 0$, transistor $Q_P$ is ‘on’ and $Q_N$ is ‘off’. The output is therefore connected to $V_{DD}$ via the small on-state resistance of pull-up transistor $Q_P$ i.e. $v_O = V_{DD} = ‘high’$.

The new operating point gives $v_o \sim V_{DD}$. The output is now connected to $V_{DD}$ via the small ‘on’ resistance of $Q_P$ which we call $r_{DSP}$. A similar analysis gives the value of $r_{DSP}$ as:

\[
r_{DSP} \approx \frac{1}{k_p \left( \frac{W}{L} \right)_p (V_{DD} - |V_{tp}|)}
\]
20.2) The Voltage Transfer Characteristic

Symmetric VTC due to the use of matched transistors. The VTC will be less symmetric if transistors are not matched.
EXERCISES

14.6 Consider a CMOS inverter fabricated in a 0.13-μm process for which $V_{DD} = 1.2$ V, $V_{in} = -V_{tp} = 0.4$ V, $\mu_n/\mu_p = 4$, and $\mu_n C_{ox} = 430$ μA/V$^2$. In addition, $Q_N$ and $Q_P$ have $L = 0.13$ μm and $(W/L)_n = 1.0$.

(a) Find $W_P$ that results in $V_M = 0.6$ V.
(b) For the matched case in (a), find the values of $V_{OH}, V_{OL}, V_{IH}, V_{IL}, NM_{IN},$ and $NM_L$.
(c) For the inverter in (a), find the output resistance in each of its two states.
(d) For a minimum-size inverter for which $(W/L)_p = (W/L)_n = 1.0$, find $V_M$.

Ans. (a) 0.52 μm; (b) 1.2 V, 0 V, 0.65 V, 0.55 V, 0.55 V, 0.55 V, 0.55 V, 0.55 V, 0.55 V; (c) 2.9 kΩ, 2.9 kΩ; (d) 0.53 V

D14.7 A CMOS inverter utilizes $V_{DD} = 5$ V, $V_{in} = |V_{tp}| = 1$ V, and $\mu_n C_{ox} = 2\mu_p C_{ox} = 50$ μA/V$^2$. Find $(W/L)_n$ and $(W/L)_p$ so that $V_M = 2.5$ V and so that for $v_I = V_{DD}$, the inverter can sink a current of 0.2 mA with the output voltage not exceeding 0.2 V.

Ans. $(W/L)_n \approx 5$; $(W/L)_p \approx 10$